CMS PHASE-2 TRIGGER UPGRADE PLANS AND R&D

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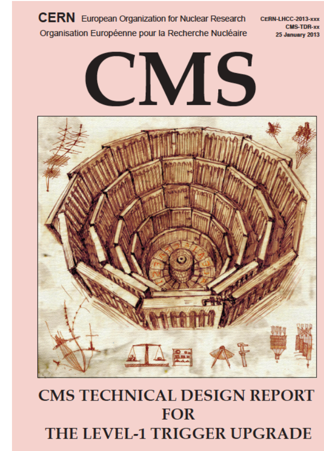
First: Phase-1 Level-1 Trigger Upgrade

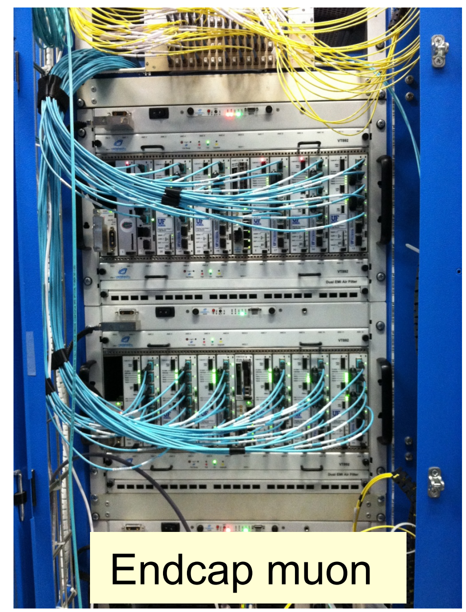
- To address the rate and pile-up challenges of LHC Runs 2 and 3, upgrade to improve:
  - e/γ and τ cluster footprints and isolation
  - Muon pT resolution and muon isolation
  - Jets and Energy sums with pile-up subtraction
  - Menu sophistication (#lines, complexity)
- A complete replacement of the Run 1 system
  - Increase system flexibility with high bandwidth optical links and large FPGAs
  - Further standardization across systems using μTCA telecomm platform
  - Build and commission upgrade in parallel with current trigger in 2015, deploy in 2016
- Designed to achieve ultimate performance without:
  - Silicon tracking at Level-1
  - Crystal granularity for electromagnetic calorimetry
  - Raising the read-out rate ceiling for FE electronics
  - Increasing the trigger latency

CERN-LHCC-2013-011

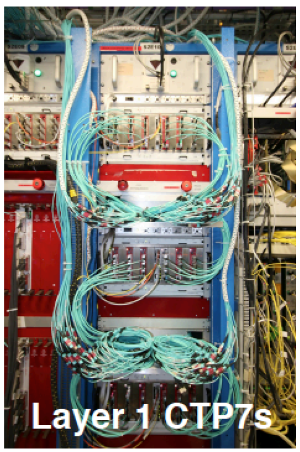

CERN European Organization for Nuclear Research
Organisation Européenne pour la Recherche Nucléaire

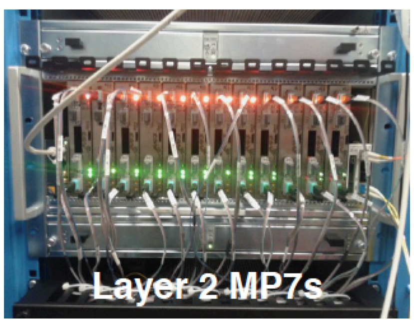
CMS

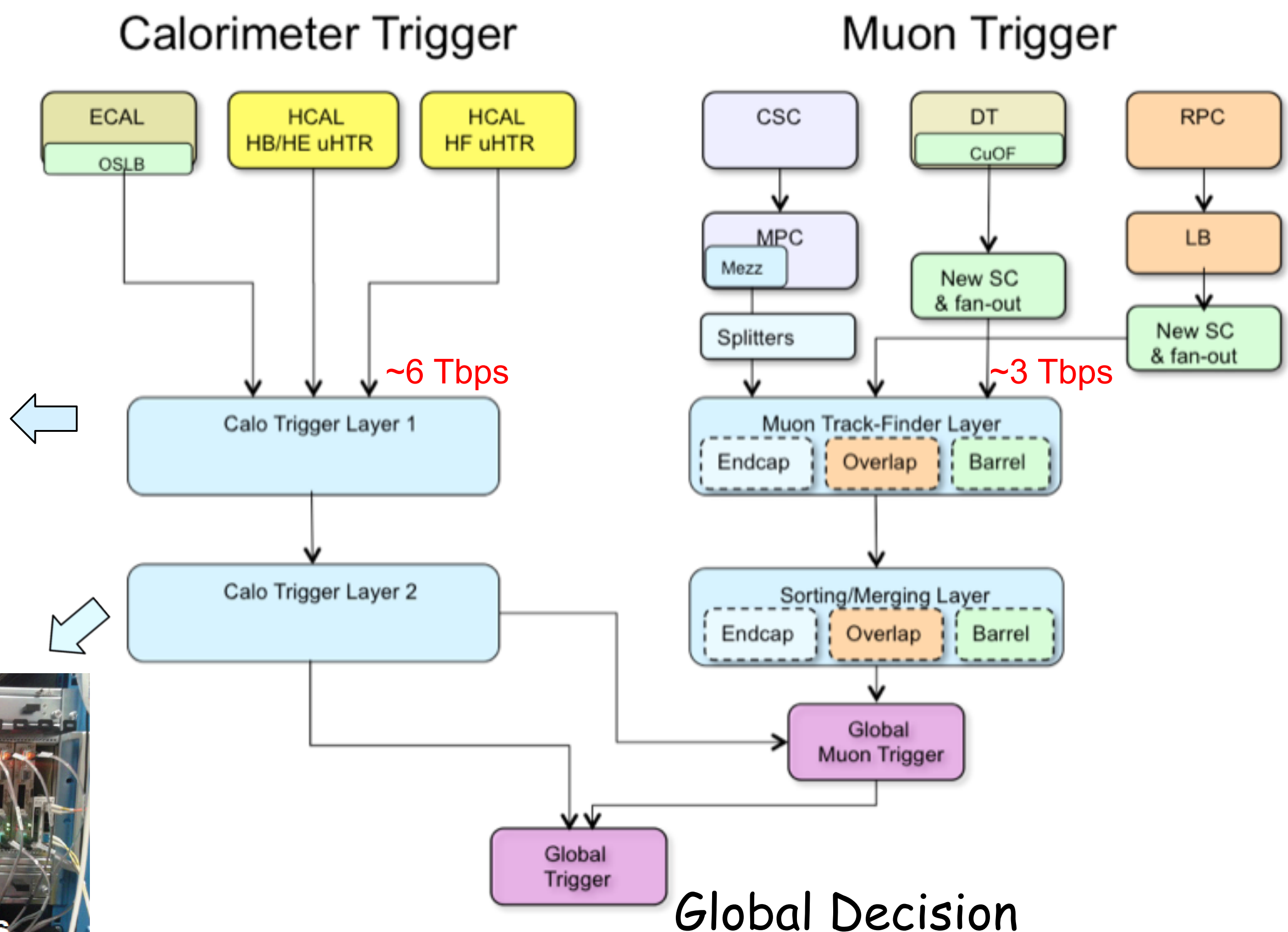
CMS TECHNICAL DESIGN REPORT
FOR
THE LEVEL-1 TRIGGER UPGRADE


Endcap muon

Phase-1 Trigger Architecture





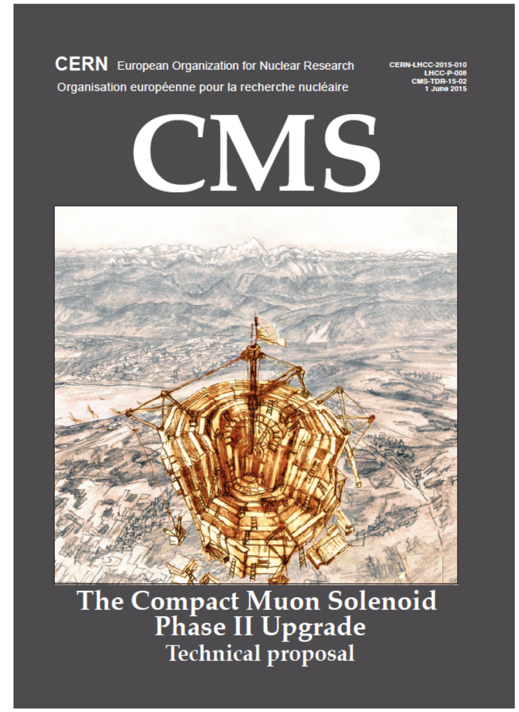


Challenges of High Luminosity LHC

- Integrated luminosity of 3000 fb^{-1} beyond LHC Run 3
  - Fully explore the electroweak sector (Higgs couplings) and reach ultimate sensitivity for TeV scale physics
- Luminosity leveled to 5×10^{34} Hz/cm^2 (pile-up ~140), possibly as high as 7.5×10^{34} Hz/cm^2 (pile-up ~200)
  - Compare to Runs 2+3: $L<2\times10^{34}$ Hz/cm^2 (pile-up ~50)
- Increased rate and pile-up effects:
  - Muon thresholds pushed into the flat region of rate curve because of limited P_T resolution
  - Very high e/gamma trigger rates
  - Degradation of the utility of calorimeter-based isolation due to high pile-up
  - Blow-up in rate of energy sum and multi-jet triggers due to high pile-up
- Nevertheless need thresholds efficient for precision electroweak scale measurements (Higgs) and TeV scale

CMS Phase-2 Upgrade for the HL-LHC

- CMS Technical proposal:
  - CERN-LHCC-2015-010
  - https://cds.cern.ch/record/2020886

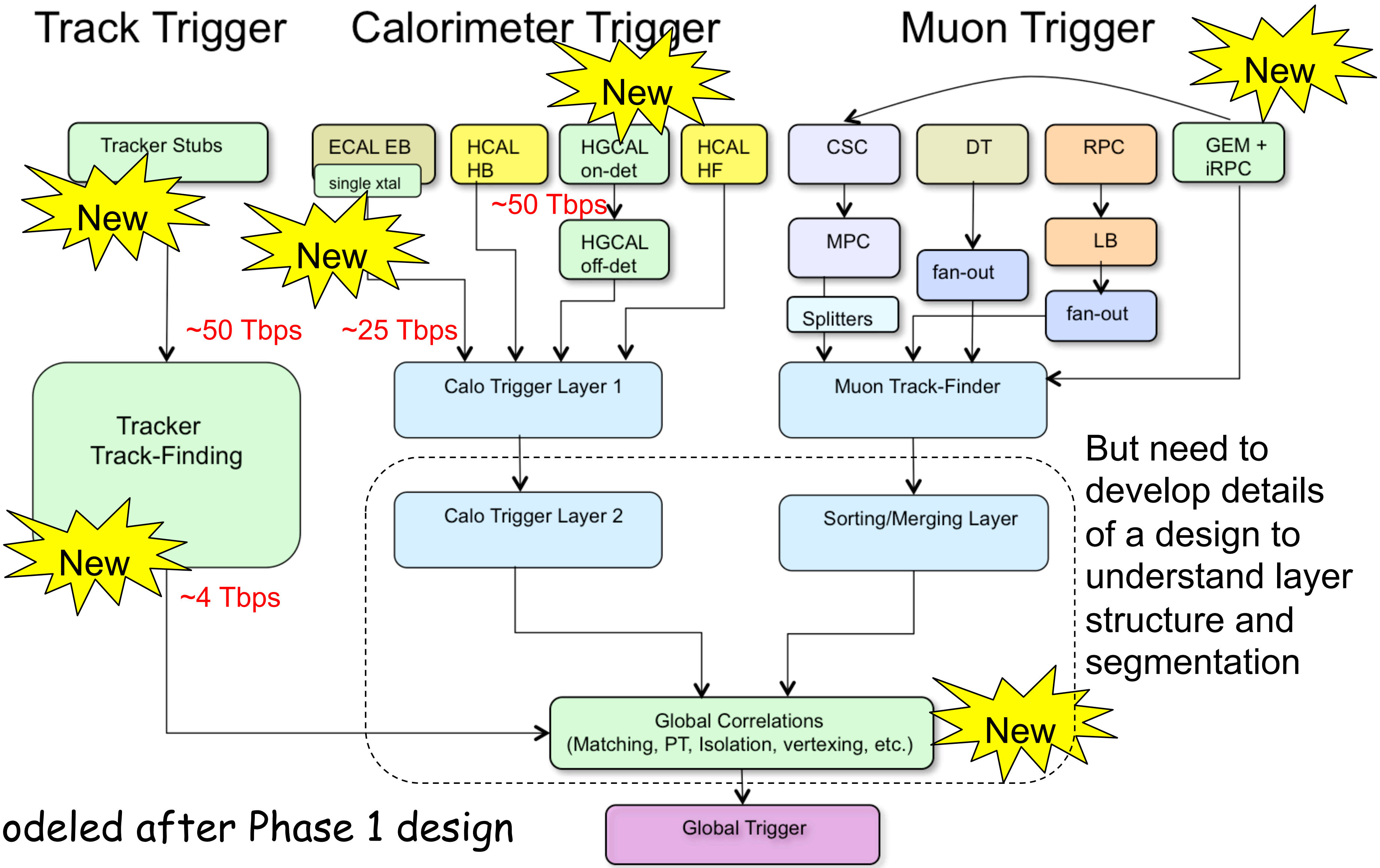


- Detector upgrades:
  - Silicon strip Outer Tracker
  - Pixel Tracker
  - Forward calorimetry
  - Forward muons
  - Bream radiation protection and luminosity
  - Trigger /DAQ

Phase-2 Level-1 Trigger & Readout Design Specifications

- Incorporation of tracking at Level-1 from the silicon tracker
  - Major missing ingredient!
- Correlation of tracks with other Level-1 objects
  - Better charged lepton ID, refine (muon) momentum, assign jet vertex, determine primary vertex, provide track-based isolation …
- Introduction of crystal granularity at Level-1 for ECAL barrel
  - $\Delta\varphi\Delta\eta = 0.0175 \times 0.0175$ vs. 0.0875×0.0875
  - Better spike rejection and EM shower identification
- Incorporation of Phase-2 forward muon detectors into muon Track-Finder trigger (GEM, iRPC)
  - Increased redundancy, more bending angles
- Trigger rates up to 750 kHz @ Level-1, 7.5 kHz @ HLT
  - Compare to today: 100 kHz and ~1 kHz
  - Alleviate a Level-1 bottleneck and allow HLT to do more
- Level-1 trigger latency of 12.5 μs (500 BX * 25ns/BX)
  - Compare to today: 4.0 μs
  - Allow time for additional processing (Track Trigger, Correlation)

A Possible Level-1 Trigger Architecture



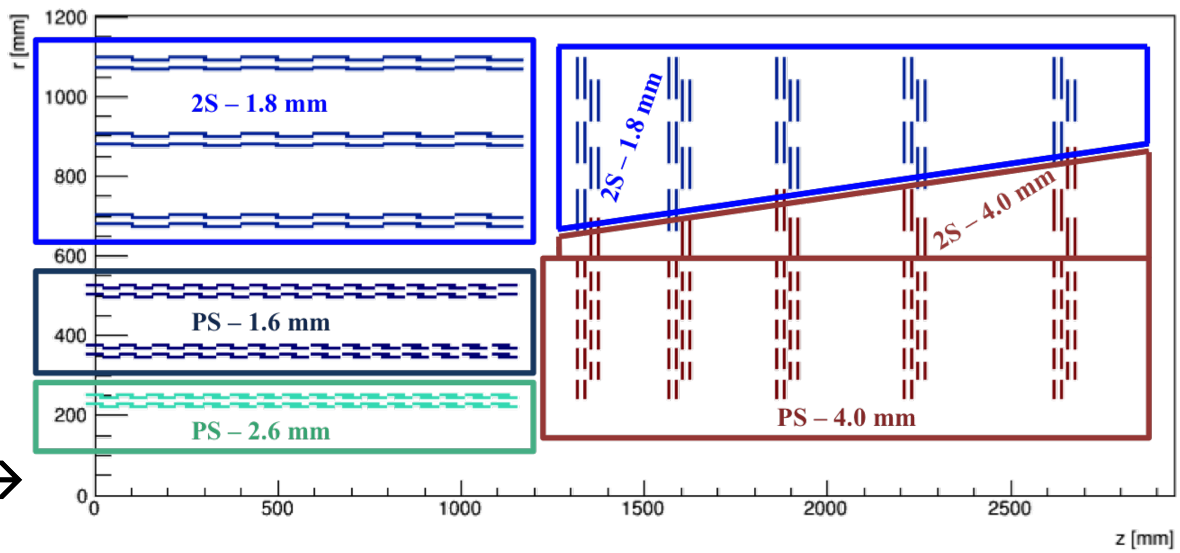
But need to develop details of a design to understand layer structure and segmentation

Modeled after Phase 1 design

Phase-2 Outer Tracker Design

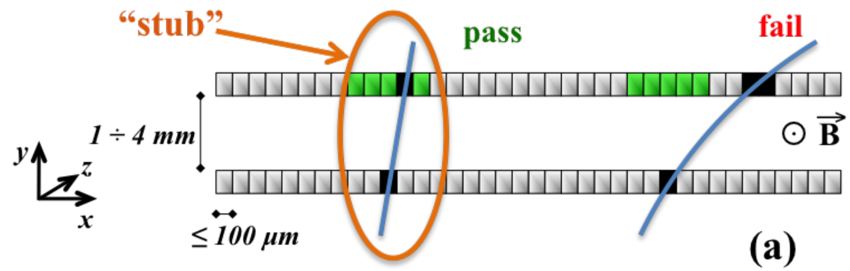
- Baseline design has 6 barrel layers and 5 endcap disks
  - 10 and 11 layers, respectively, in current Tracker
  - 220 m^2 area
- Two sensor modules in all layers for triggering (stubs)
  - 2S: 2.5cm strips, 90μm pitch
  - PS: Long Pixel (1.5mm) in 3 inner layers for z-coordinate, and 5cm strips, 100μm pitch
  - 50M strips
  - 220M macropixels
  - Sensor spacing optimized to obtain 2 GeV p_T threshold

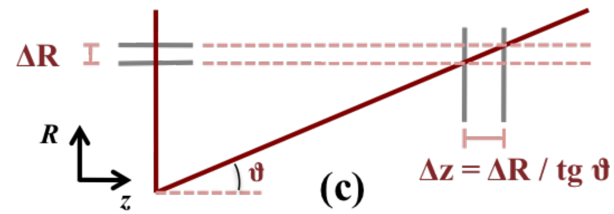
Inner pixels not shown →



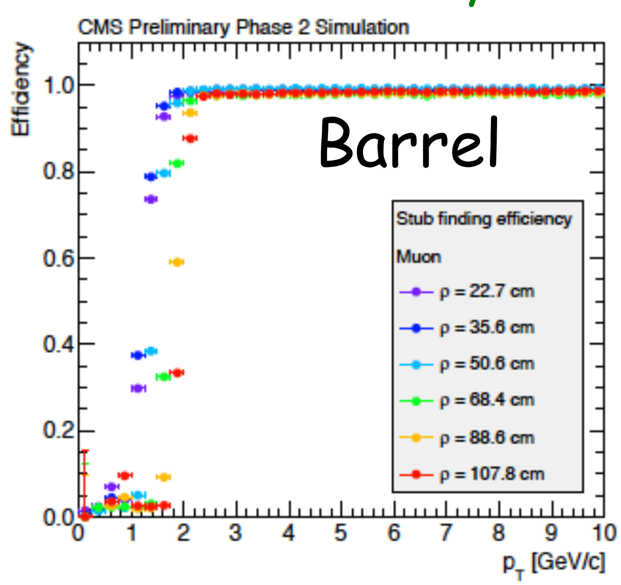
Track Stub Finding

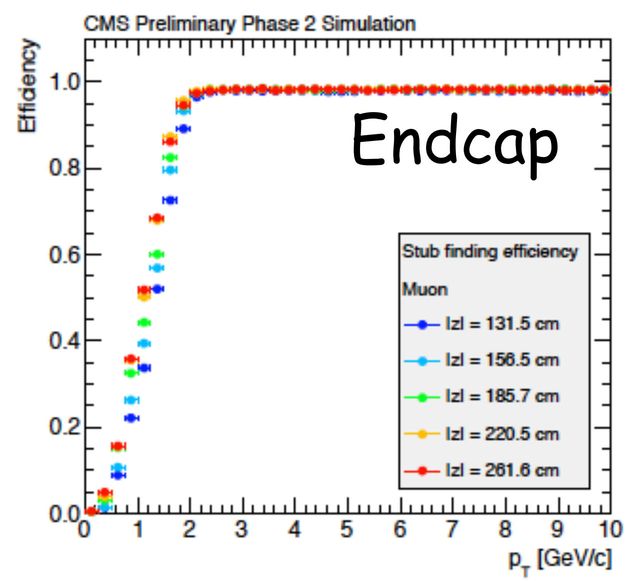
- Double layers help reduce data bandwidth.
- Require a coincidence within a road, limits $P_T > 2$ GeV
  - < 3% of tracks
- "Push" design: all stubs forwarded
  - 3-4 stubs/module/BX for Barrel layer 1
  - ~10K stubs/BX
  - O(50) Tbps





Stub efficiency vs. P_T for various layers and disks →





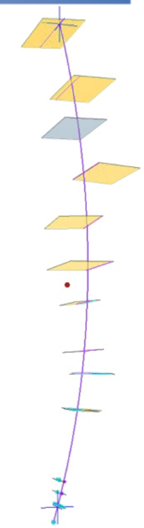
1 BX = 25ns

Track-Finding

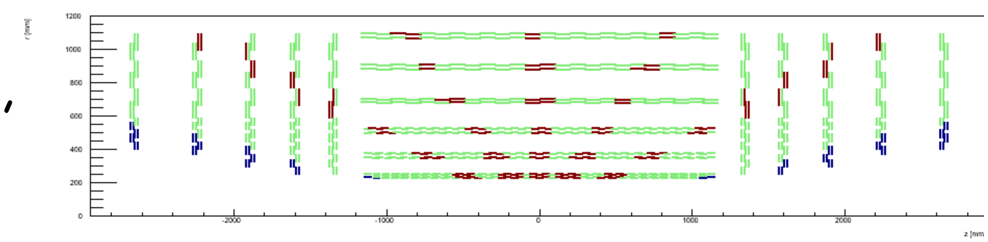
More in T.Liu's and A.Ryd's reports

- Again a "push" design, not region of interest
  - Input: Expect ~10K stubs/BX @ PU~140, of which 5-10% belong to tracks with P_T>2 GeV
  - Output: ~100 bits/track → several Tbps to track correlators
  - Latency: ~5 μs allocated
- Multiple approaches under consideration to find tracks:
  - Pattern-based: Track patterns stored in Associative Memory chips
    - Target implementation in custom ASICs to store large number of patterns (~100M overall)
  - Hough transform: transformation of track patterns to clusters in transformed space
    - Target implementation in FPGAs
  - "Tracklet" approach: Track building from stubs with pair-wise layer extrapolations
    - Target implementation in FPGAs
- Generally implemented with time-multiplexing of the input data (round-robin of event data to processors)
- All followed by a track-fitting stage to extract track parameters

Pattern Recognition with AM Approach



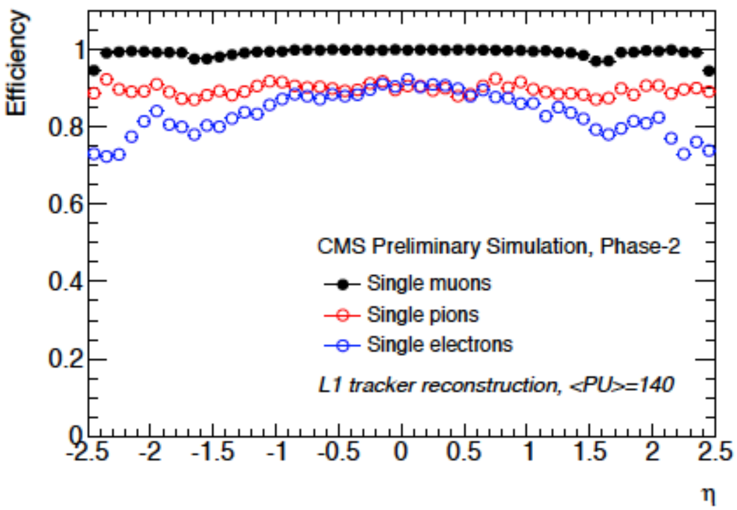
- Identify track patterns from hits across different detector layers
  - Content addressable memory cells with provision for majority logic in pattern
  - Generally does well for high occupancy environments
  - Massively parallel approach
- CMS AM Track-Trigger Concept
  - Partition geometry into 48 towers (6 in $\eta \times 8$ in φ)
  - Target:

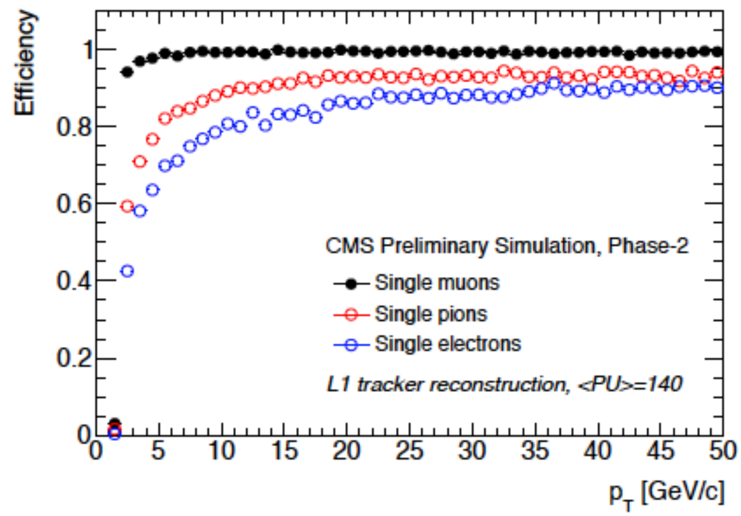


    - 1 ATCA crate per tower, with 40 Gbps full mesh backplane (Time MUX)
    - ~2M patterns per tower
    - ~200K patterns/AM chip
      - ➡ Ultrascale FPGA for current prototype
      - ➡ Develop ASIC prototypes in 2D (~2018) and 3D (~2021)

Track-Finding Performance

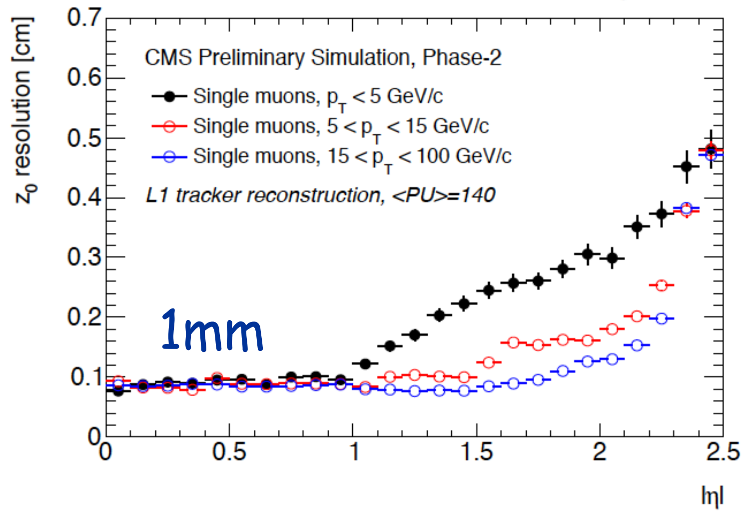
- Efficiency curves vs. eta and PT for PU=140:





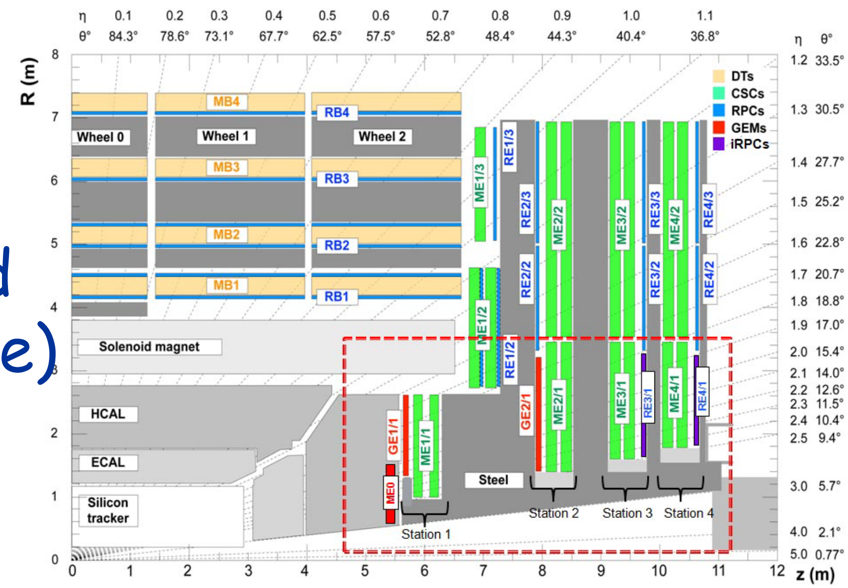
Tracklet approach

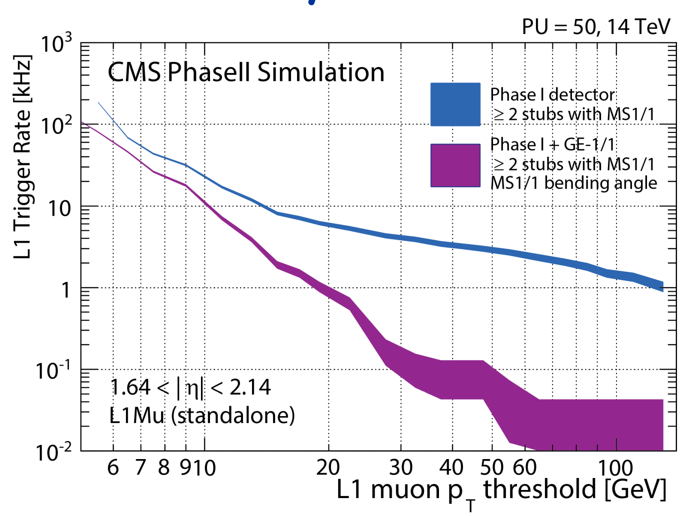
- Z0 resolution:



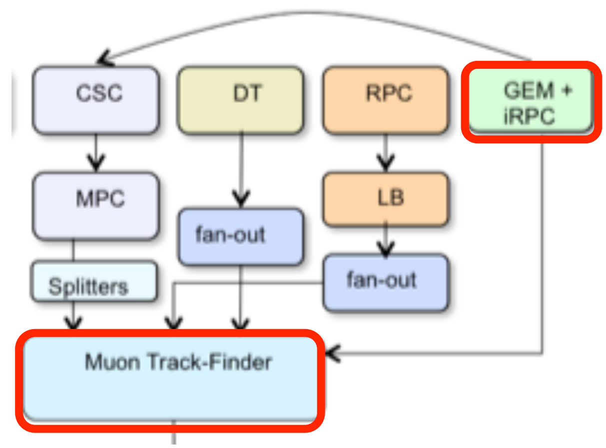
Standalone Muon Trigger

- New detectors in forward region to add redundancy and enhance trigger
  - GEM in first 2 layers
  - Improved RPC in outer layers
- Additional inputs and improved angular information (bend angle) for track-finding for better efficiency and rate rejection



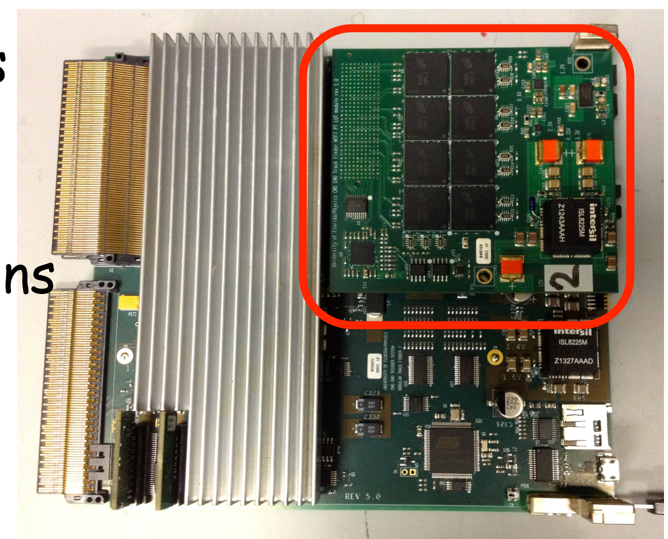


Rate just in GE1/1 region

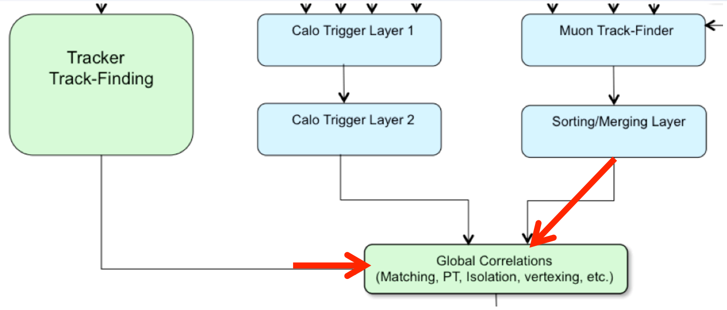


Example from Phase 1 Upgrade

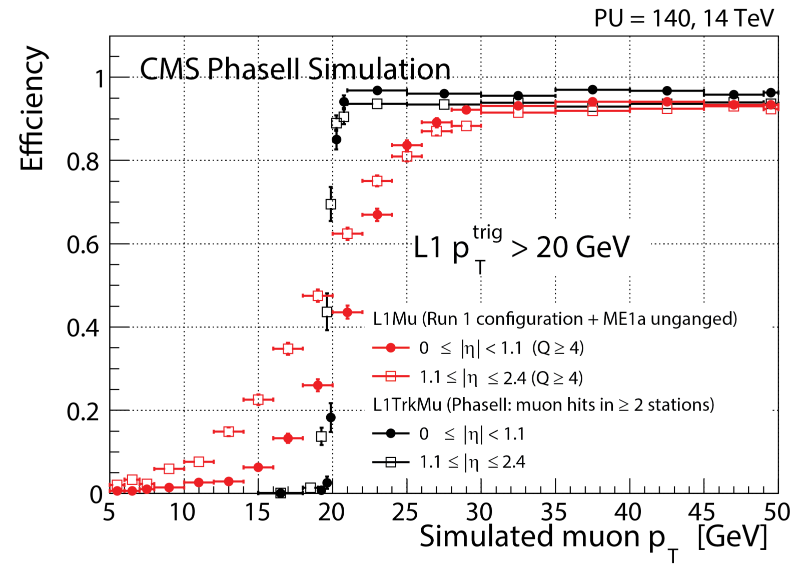
- Muon rate reduction comes from improved P_T resolution
- Large look-up table has been very successful for the muon PT assignment at Level-1 in CMS forward region
  - Non-uniform B-Field
  - Ability to use multiple deflection angles in φ and η within and between measurement layers
  - Phase-1 making use of Boosted Decision Trees for calculation
- 4MB (legacy) → 1 GB for Phase 1 upgrade LUT
  - Memory type: Micron RLDRAM3
    - Total size: 1G x 9 bits, 30 address bits
      - ➡ Upgradeable in future
    - Clock frequency: 200 MHz
    - Random address read operations: 5/25ns
    - Latency: 2 LHC clocks
    - Memory array is split into 32M banks, 32 words each



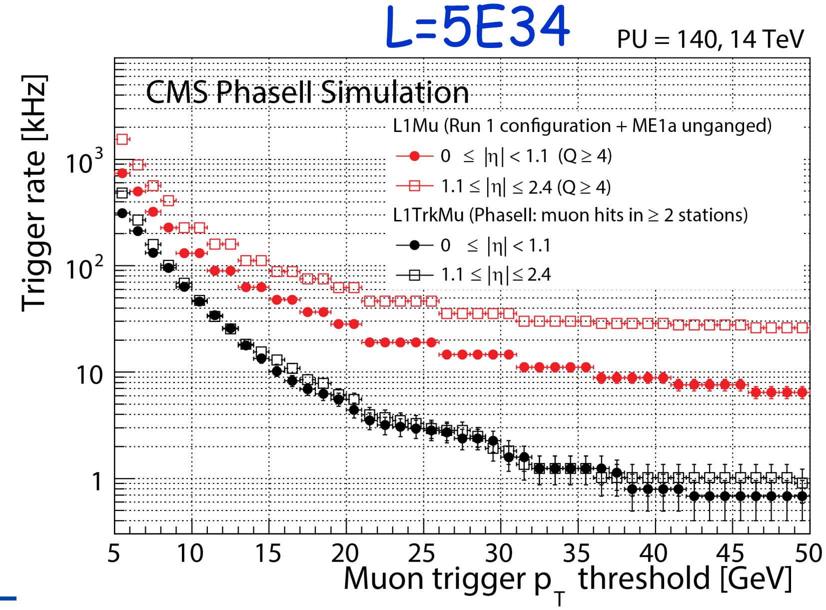
Muon-Track Correlation



- Match standalone muons to tracker tracks, take measurements from track
  - P_T resolution improves from O(20%) to 1-2%
- Sharpens turn-on efficiency
- Drops rate ~10X from current 2015 muon trigger
  - However, closer to ~5X rate reduction after 2016 Phase 1 muon upgrade



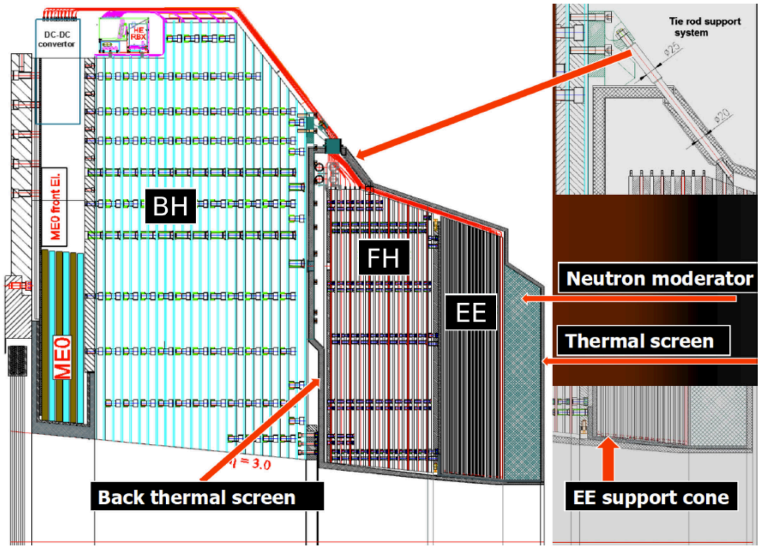
L=5E34



High Granularity Calorimeter (HGC)

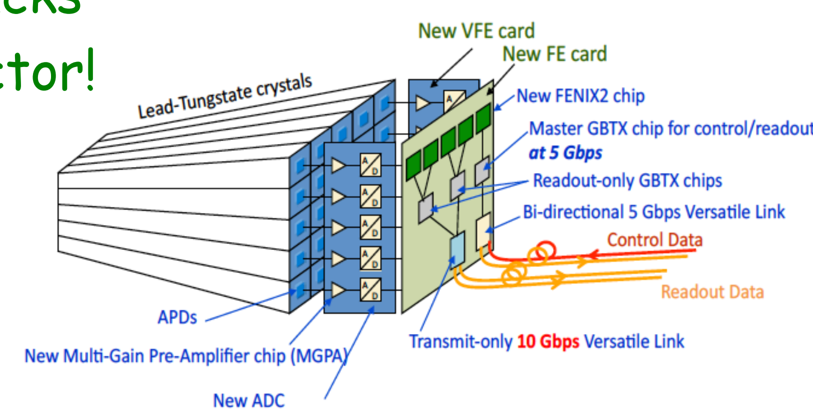
- New endcap calorimeter with high granularity to survive radiation does and high pile-up environment of HL LHC (inspired by ILC detector design)
  - Electromagnetic (EE): 28 layers of silicon/tungsten
  - Front Hadronic (FH): 12 layers of silicon/brass
  - Back Hadronic (BH): 12 layers of scintillator/brass

  589 m^2
  6.1M ch.
- Trigger primitives:
  - 850K sums for EE+FH @ 40 MHz transferred off detector
    - 2x2 sensor pads, alternate active planes, each 2 x 10 Gbps links → O(50) Tbps transferred
      - Comparable to tracker output
  - Form longitudinal clusters and projective towers in off-detector electronics



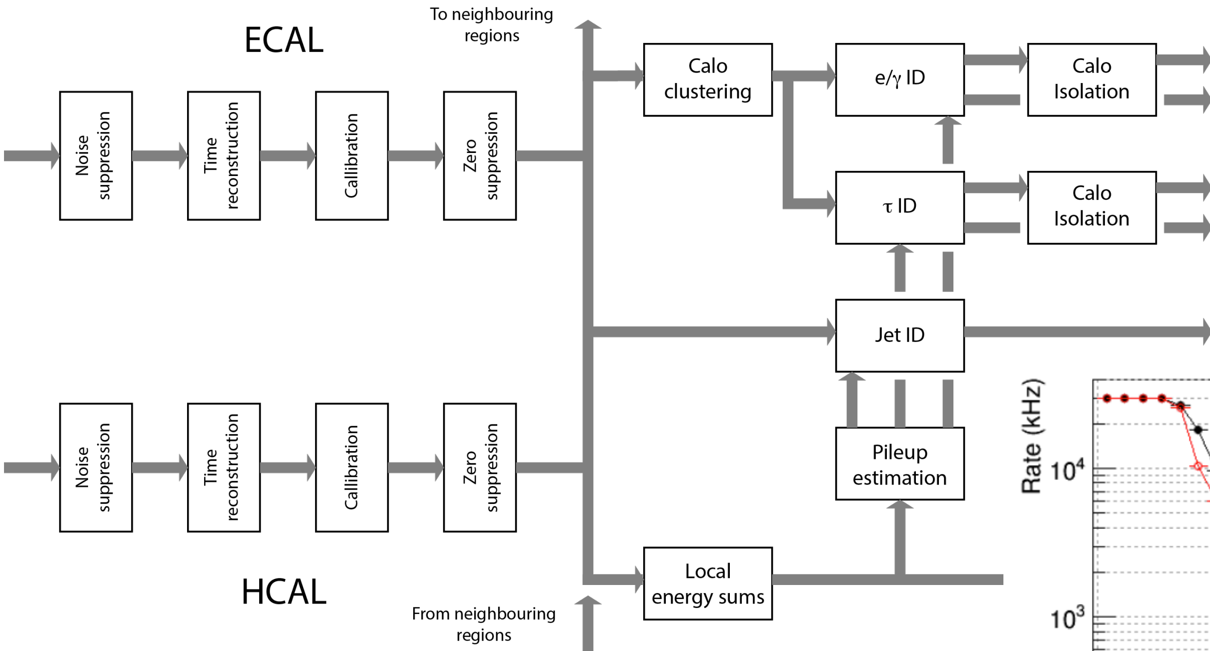
ECAL Barrel Trigger Primitives

- In order to meet the requirements for an L1 rate of 750 kHz and a latency of 12.5 μs requires a redesign of the ECAL barrel front-end electronics
- Take opportunity also to deliver trigger information at crystal granularity (vs. 5x5 currently)
  - Utilize newer rad tolerant link technology for O(10) Gbps/ch.
  - Improves spike rejection in single APD channel from hadron interaction in APD (energy comparison to 4 neighbors)
  - $\Delta\varphi\Delta\eta = 0.0175 \times 0.0175$ (vs. 0.0875×0.0875) better granularity to match to tracks
  - O(25) Tbps transferred off detector!
    - Comparable to Tracker output



Calorimeter Trigger

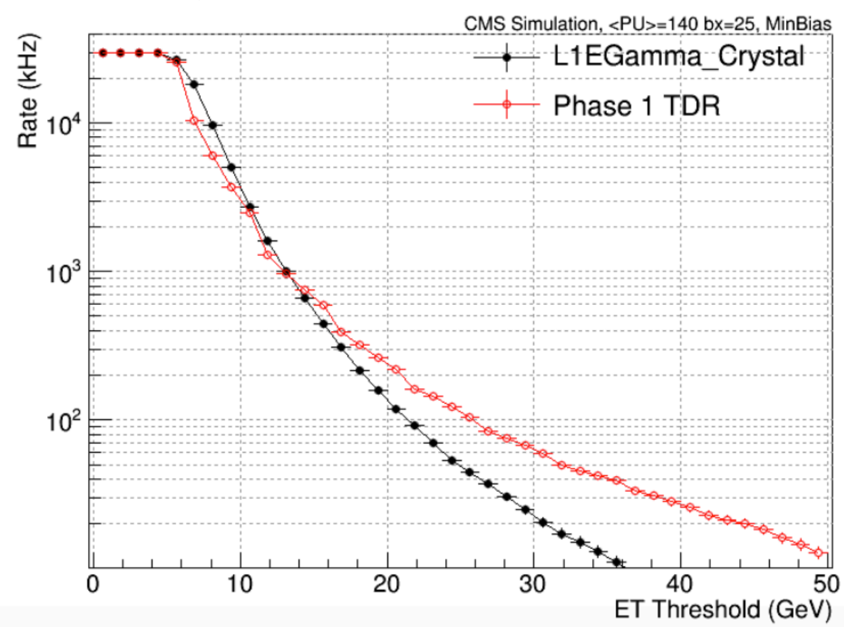
- Cluster energies into electron/photons, taus, jets, and form energy sums (H_T, E_T^{miss}, total E_T)



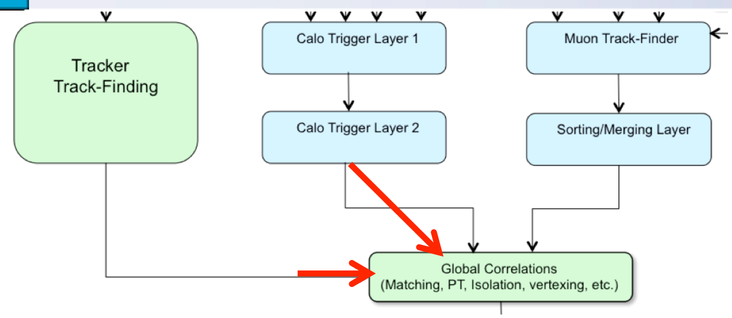
← Processing workflow

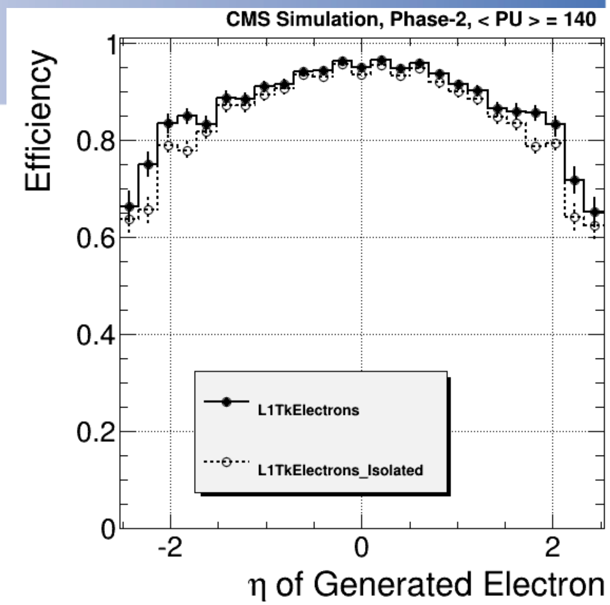
Barrel e/γ rate vs. ET for single xtal resolution vs. 5x5 →

2 – 3X rate reduction

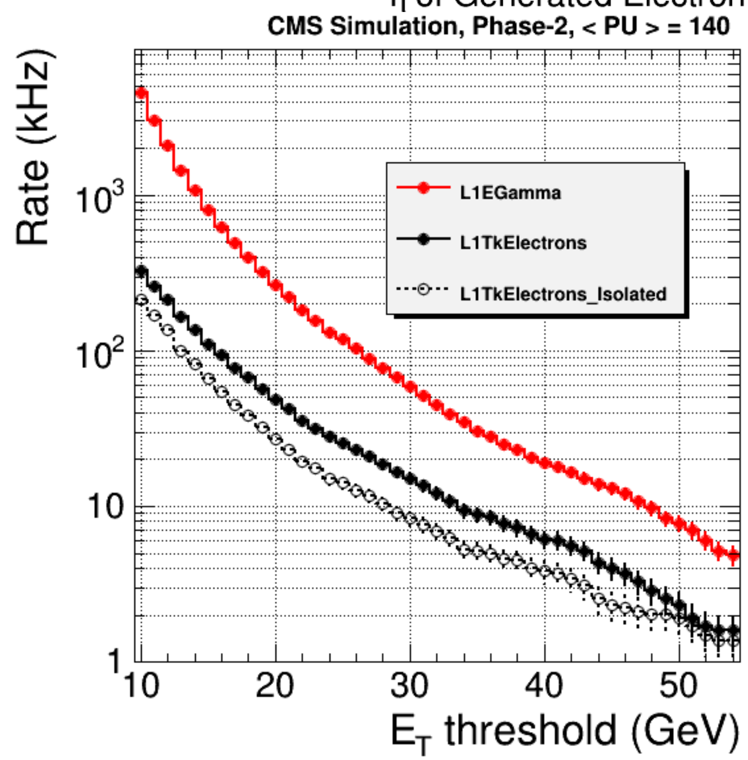


Electron-Track Correlation



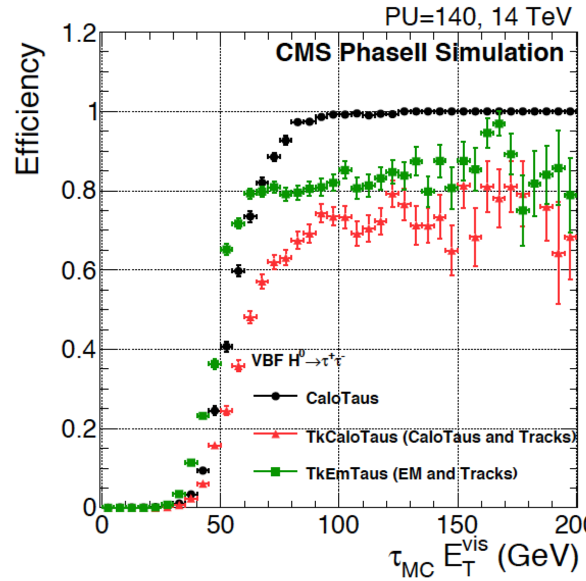


- Match EG objects to tracker tracks
  - Reduced track efficiency compared to muons from material interaction
- Drops rate ~5X for E_T>20
  - ~2X after single xtal improvement
- Track isolation
  - Tracks in cone about lepton with consistent z0
  - Cut on relative isol: $\Sigma P_T^{trk} / P_T^e$
  - Rate reduction ~2X



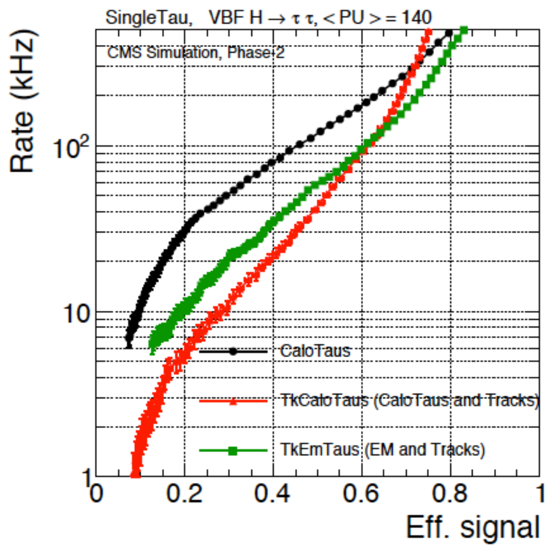
Tau Track Triggers

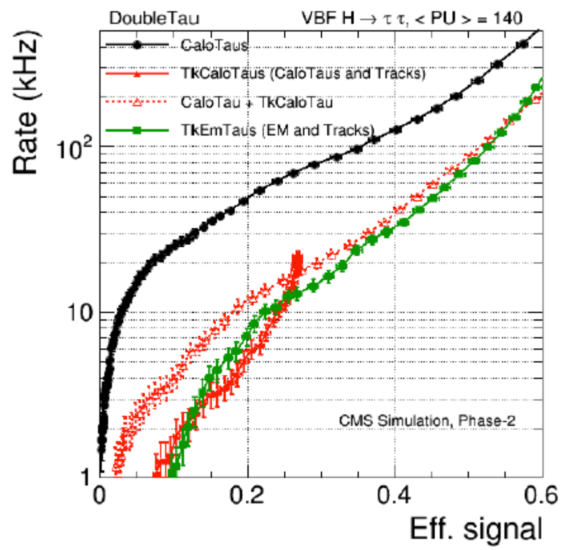
- Two approaches studied:
  - Matching calo tau objects with track
    - High quality track in narrow cone with P_T>15 and no other tracks in isolation cone
  - Matching tracks to e/γ clusters
    - Combine high quality tracks with consistent z0 and e/γ clusters with E_T>5 with inv. mass < m_τ



Rate vs. VBF H→ττ effic. for single (left) and double (right) tau triggers

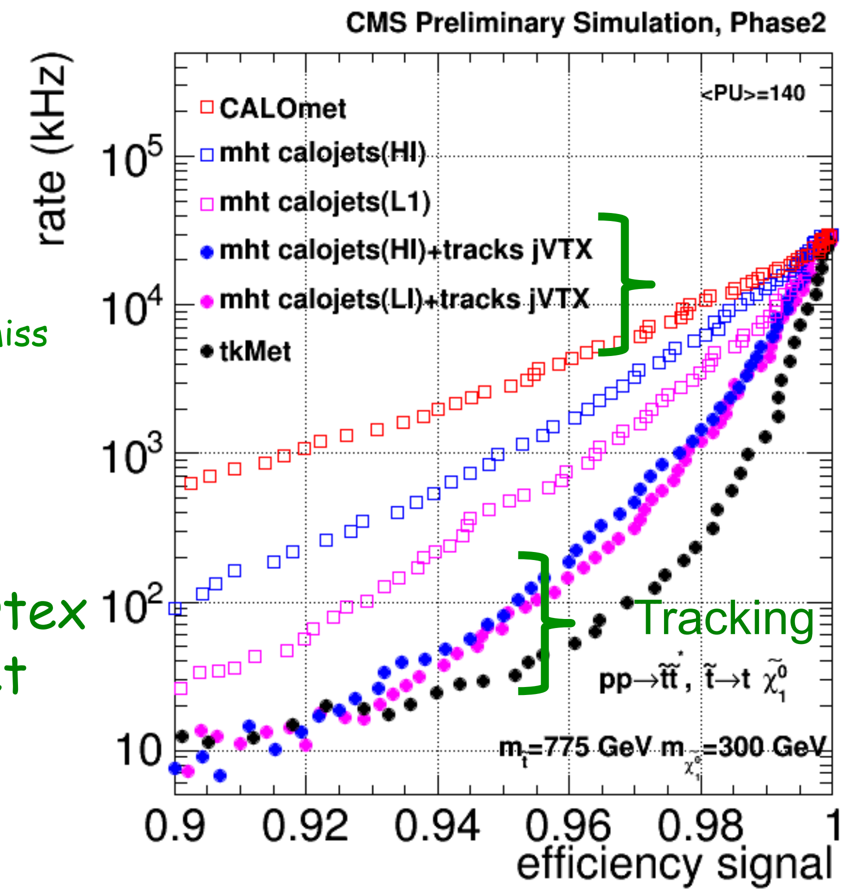
Rate reduction ~2X with tracking (~50 kHz @ 50%)





Energy Flow with Tracks

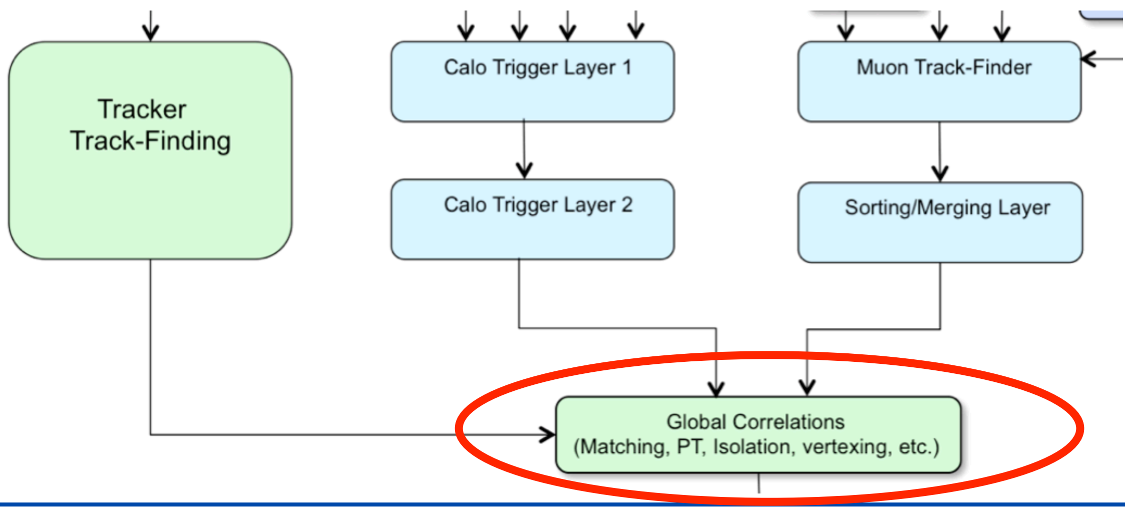
- Event vertex
  - Resolution ~5mm for tracks with P_T>2
- Jet-vertex matching
  - Energy sums such as H_T and H_T^{miss} purely based on calorimeter quantities are very sensitive to pile-up
  - Requiring consistency with a vertex greatly improves multijet and jet sum triggers
- Track-based MET
  - Reconstruct missing transverse momentum from tracks associated to primary vertex
    - Less affected by pile-up



Impact of several triggers with and without tracking for a SUSY scenario

Particle Flow at Level-1?

- Full exploitation of tracking at Level-1
  - Requires matching all calorimeter clusters to all tracks, removing clusters not attached to the primary vertex, and replacing cluster energy with track parameters for rest
  - Significantly improves the jet and hadronic energy flow measurements at CMS. Also reduces pile-up dependence.
  - Very successful in offline reconstruction and at HLT
- Likely very ambitious for Level-1…



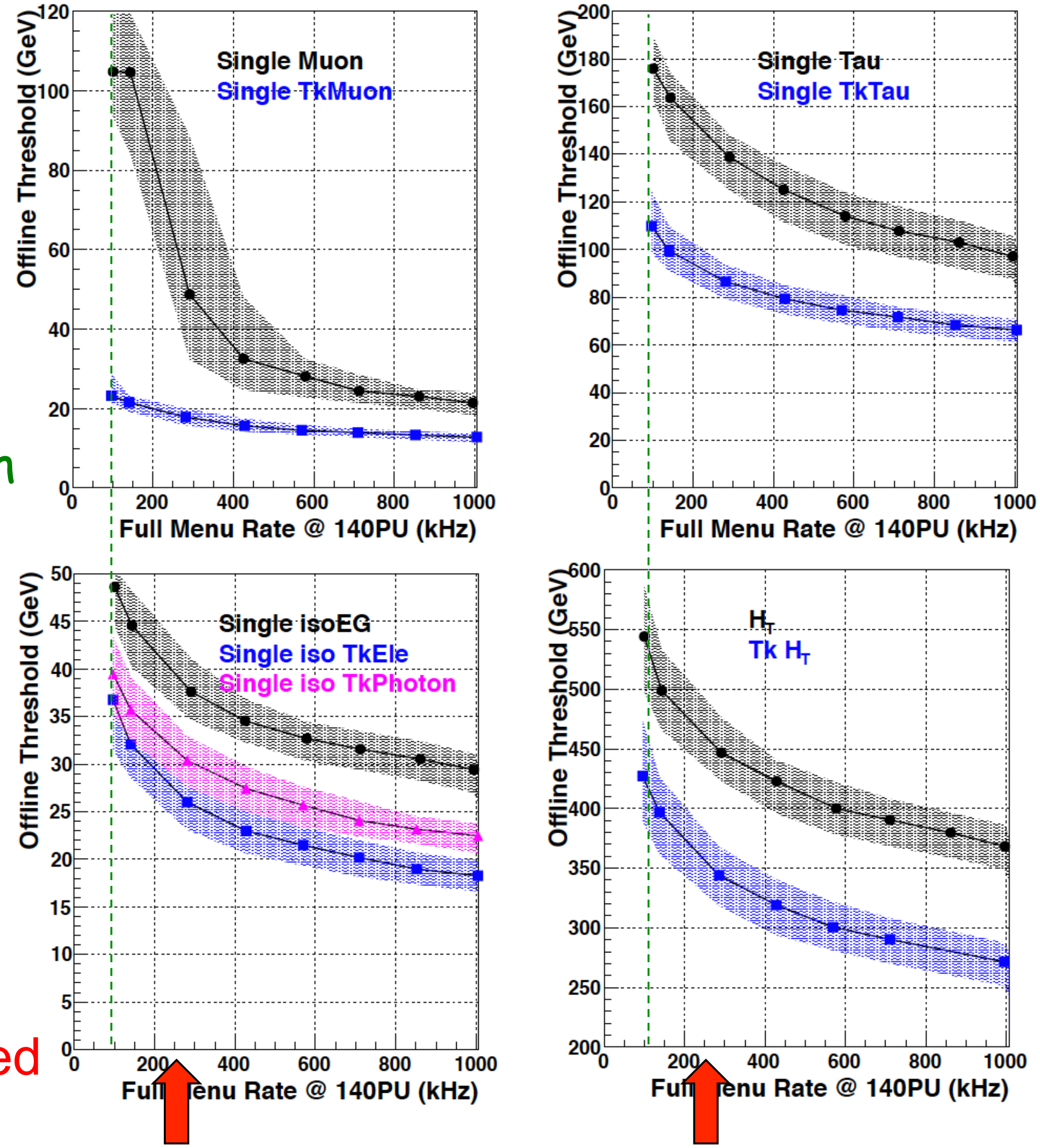
Simplified Example Level-1 Trigger Menu

- Target L = 5.6E34, PU=140
  - Main track-based triggers
  - Thresholds are comparable to Phase 1 as intended
  - Estimate 30% of rate missing to all other cross triggers
  - 260 kHz @ PU=140
- Scales to 500 kHz @ PU=200
  - Then add safety factor of 1.5 → design for 750 kHz ultimate rate from Level-1

$L = 5.6 \times 10^{34}$ cm^{-2}s^{-1} $\langle PU \rangle = 140$	Level-1 Trigger with L1 Tracks	
Trigger Algorithm	Rate [kHz]	Offline Threshold(s) [GeV]
Single Mu (tk)	14	18
Double Mu (tk)	1.1	14 10
ele (iso tk) + Mu (tk)	0.7	19 10.5
Single Ele (tk)	16	31
Single iso Ele (tk)	13	27
Single γ (tk isol)	31	31
ele (iso tk) + e/γ	11	22 16
Double γ (tk isol)	17	22 16
Single Tau (tk)	13	88
Tau (tk) + Tau	32	56 56
ele (iso tk) + Tau	7.4	19 50
Tau (tk) + Mu (tk)	5.4	45 14
Single Jet	42	173
Double Jet (tk)	26	2@136
Quad Jet (tk)	12	4@72
Single ele (tk) + Jet (tk)	15	23 66
Single Mu (tk) + Jet (tk)	8.8	16 66
Single ele (tk) + H_T^{miss} (tk)	10	23 95
Single Mu (tk) + H_T^{miss} (tk)	2.7	16 95
H_T (tk)	13	350
Rate for above Triggers	180	
Est. Total Level-1 Menu Rate	260	

Dependence of Trigger Threshold vs. Total L1 Bandwidth

- Illustrates benefit of tracking
- Thresholds obviously can be reduced with more L1 bandwidth
  - Note current bandwidth limit is 100 kHz
- Diminishing returns beyond 750 kHz



Bandwidth assumed for previous menu

HLT

More on DAQ in R.Mommsen report

- If we have full tracking at Level-1, what is left for HLT to achieve another factor 100 reduction in rate?
- Tracking
  - Has access to pixel hits in addition to strips → b-tagging
  - HLT so far has not had the resources to perform global tracking for the entire Level-1 bandwidth
  - But with the Track-Trigger, the full collection of tracks can be accessed by HLT for every event and used even if Level-1 did not need to for all triggers to achieve rate reduction
    - Like FTK for ATLAS trigger
- Particle Flow
  - As mentioned, maximally combining tracking with calorimetry greatly improves performance of jet and energy sum triggers
  - Likely that HLT would be much closer to offline performance than what could be possibly achieved at Level-1

Milestones for Phase-2 Trigger

Milestone Identifier	Target date	Description
TP.L1.1	Q2 2016	Initial definition of trigger algorithms, primitive objects, and inter-layer objects
TP.L1.2	Q4 2016	Initial demonstration of key implementation technologies
TP.L1.3	Q2 2017	Baseline definition of trigger algorithms, primitive objects and interchange requirements with subdetectors
TP.L1.4	Q4 2017	Software emulator demonstrates implementation of core phase 2 trigger menu with baseline objects
TP.L1.5	Q1 2018	Definition of hardware technology implementation baseline
TP.L1.6	Q4 2018	Full-function prototypes produced which allow local comparison with emulator
TP.L1.7	Q4 2019	Demonstrator system shows integration and scaling, global/full-chain comparison with emulator
TP.L1.8	Q1 2020	Phase 2 Trigger TDR

Demonstrators in 4 years

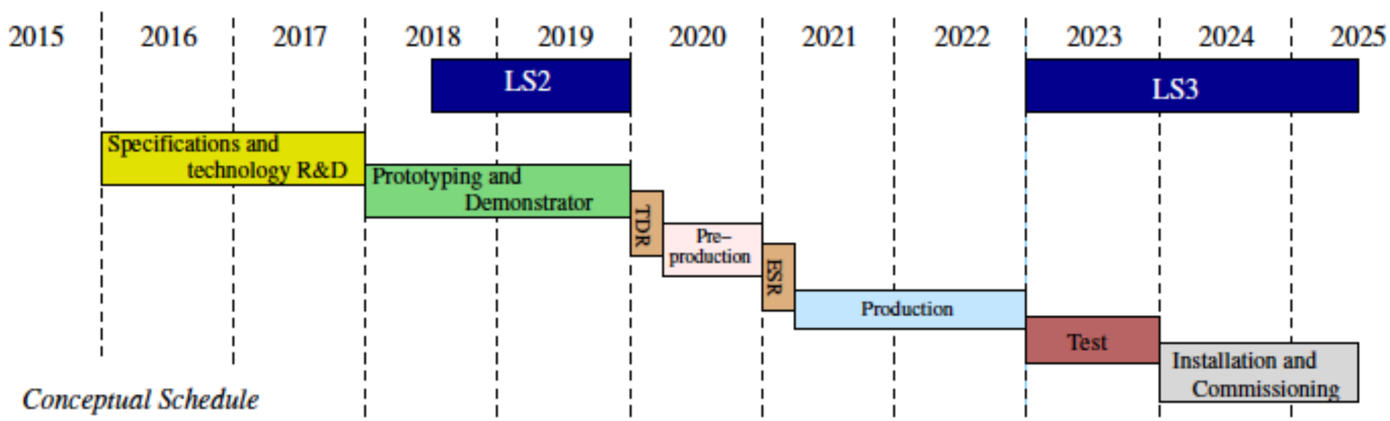


Figure 6.17: Conceptual schedule for the Trigger Phase-II upgrade.

Trigger Electronics R&D Directions, 1

- I/O bandwidth and system/PCB design
  - Electronic systems designed to handle O(50) Tbps input
  - High bandwidth optical data links at O(25) Gbps
  - High bandwidth backplane communication
- Logic implementation
  - Ultrascale FPGAs
    - And associated high-level synthesis tools to improve productivity
  - Associative Memory ASIC, 3D technology for high density
- Large, fast memory access
  - Access to >GB memory *near logic resources* for quick, complex calculations via large lookup table (P_T assignment in tracking triggers)

Trigger Electronics R&D Directions, 2

- Electronic controls
  - Clock and trigger control signal distribution to systems
  - On-board processors (e.g. Xilinx ZYNC) for board control and monitoring
- Platform technologies
  - Evaluate platforms for backplane bandwidth, card real estate, power density …
  - xTCA? (Telecommunications Architecture)
    - CMS Phase-1 upgrade electronics are based on μTCA standard
    - Advanced TCA for some Phase 2 implementations?

Note: important to maintain ties with industry as well as ECE colleagues at universities on technology and tool developments

Summary

- CMS has an ambitious but achievable program to upgrade its detectors and the Level-1 Trigger electronics for HL-LHC
  - For the Level-1 (HLT) Trigger, the goal is to maintain sensitivity for electroweak and TeV scale physics with rate < 750 (7.5) kHz and 12.5 μs latency
  - Bring more of what was done at HLT to the Level-1 Trigger
- Initial algorithms demonstrate meeting goal, but much more R&D required for implemented algorithms and system design
  - Likely performance can improve further (e.g. particle flow at Level-1)
- Many Level-1 trigger subsystems will absorb many tens of Tbps data input
  - Order of magnitude higher than current Phase-1 upgrade
- Trigger logic similarly expands by a large factor
  - e.g. tracking logic for the silicon detector trigger
- Need to achieve this during the next decade within roughly the same budget and overall system size as for the current Level-1 trigger system